

In th Claims

CLAIMS

Underlines indicate insertions and ~~strikeouts~~ indicate deletions.

1-50 (Cancelled).

51. (Previously Amended) An integrated circuit comprising:

a semiconductive substrate;

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a plurality of diffusion regions formed within the substrate, the diffusion regions and substrate forming junctions;

a plurality of conductive lines formed over the substrate and respective diffusion regions, the conductive lines having a generally uniform lateral width, and a portion of the conductive lines over the respective diffusion regions comprising an entirety of the lateral width of the conductive lines received directly over the respective diffusion regions, each conductive line comprising a pitch relative to an adjacent conductive line wherein the pitches are equal; and

wherein the junctions are configured to be reverse biased to preclude electrical shorting between the conductive lines and the substrate for selected magnitudes of current provided through the conductive lines.

52. (Previously Amended) The integrated circuit of claim 51 wherein each diffusion region comprises a portion disposed outwardly from directly beneath respective conductive lines.

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53. (Previously Amended) The integrated circuit of claim 51 wherein each diffusion region comprises two portions disposed outwardly from directly beneath respective conductive lines.

54. (Previously Amended) The integrated circuit of claim 51 wherein each diffusion region comprises two portions disposed outwardly from directly beneath respective conductive lines, a first portion outward of a first side of the conductive line and a second portion outward of a second side of the conductive line.

55. (Currently Amended) An integrated circuit comprising:

a semiconductive substrate;

a diffusion region formed within the substrate, the diffusion region and substrate forming a junction;

a conductive line formed over the substrate and the diffusion region, the conductive line comprising an entirety of a lateral width directly over the diffusion region;

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until
a conductive material interconnecting the conductive line and the diffusion region, an entirety of the conductive material received directly over the diffusion region; and a portion of the entirety of the conductive material laterally spaced from the conductive line; and

wherein the diffusion region is configured to be reverse biased to preclude electrical shorting between the conductive line and the substrate through the conductive material for selected magnitudes of current provided through the conductive line.

56. (Previously Added) The integrated circuit of claim 55 wherein the diffusion region comprises a portion disposed outwardly from directly beneath the conductive material.

57. (Previously Added) The integrated circuit of claim 55 wherein the diffusion region comprises at least two portions disposed outwardly from directly beneath the conductive material.

58. (Previously Added) The integrated circuit of claim 55 wherein the conductive material comprises metal.

59. (Currently Amended) An integrated circuit comprising:

a semiconductive substrate;

a diffusion region formed within the substrate, the diffusion region and substrate forming a junction;

a conductive line formed over the substrate and the diffusion region;

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could*
a conductive material interconnecting the conductive line and the diffusion region, a first portion of the conductive material received directly over the conductive line, and an entirety of the first portion of the conductive material received directly over the diffusion region;

wherein the diffusion region is configured to be reverse biased to preclude electrical shorting between the conductive line and the substrate through the conductive material for selected magnitudes of current provided through the conductive line; and

wherein the diffusion region comprises at least two portions disposed outwardly from directly beneath the combined cross-sectional area of the conductive material and the conductive line, and wherein a second portion of the conductive material contacts the diffusion region at only one location.

Claims 60-61 (Cancelled).

62. (Previously Added) The integrated circuit of claim 59 wherein the conductive material comprises metal.

63. (Previously Added) The integrated circuit of claim 51 wherein the conductive lines comprise substantially equal lateral widths.

64. (Previously Added) The integrated circuit of claim 51 wherein the conductive lines comprise equal lateral spacing between adjacent conductive lines from a perspective defined by a plane generally parallel to an upper surface of the semiconductive substrate.

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Claim 65 (Cancelled).

66. (Previously Added) The integrated circuit of claim 55 wherein the conductive line comprises at least two conductive layers.

67. (Previously Added) The integrated circuit of claim 55 wherein the conductive line comprises two conductive layers, one conductive layer directly over the other conductive layer.

68. (Previously Added) The integrated circuit of claim 55 wherein the conductive line comprises opposite sides extending from the semiconductive substrate, and further comprising sidewall spacers adjacent respective sides.

69. (Previously Added) The integrated circuit of claim 59 wherein the conductive line comprises at least two conductive layers.

70. (Previously Added) The integrated circuit of claim 59 wherein the conductive line comprises two conductive layers, one conductive layer directly over the other conductive layer.

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71. (Previously Added) The integrated circuit of claim 59 wherein the conductive line comprises opposite sides extending from the semiconductive substrate, and further comprising sidewall spacers adjacent respective sides.

72. (New) The integrated circuitry of claim 51 wherein the conductive lines have the generally uniform lateral width along their respective entireties.

73. (New) The integrated circuitry of claim 51 further comprising:
an insulative layer formed over the plurality of diffusion regions and the plurality of conductive lines; and

contact openings formed through the insulative layer and over at least three of the plurality of conductive lines, the contact openings formed along a straight line.

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and

74. (New) The integrated circuitry of claim 51 further comprising:

an insulative material formed over the plurality of diffusion regions and the plurality of conductive lines; and

contact openings formed through the insulative layer and over every other conductive line.
